Position Title	PhD Studentship in Frequency Synthesis in Networks of Phased-Locked Loops and Delay-Locked Loops
Project Abstract	The fifth generation (5G) of wireless communications is a leading- edge research topic, which has attracted increasing attention over past few years, accelerating the development of networks and low-power devices for communication. Proposed carrier frequencies for 5G communications will lie in the millimetre-wave band (e.g., 28 GHz) where the spectrum is less crowded and greater bandwidths are available. These carrier frequencies correspond to wavelengths of 1 cm and below, requiring an antenna size less of than 2.5 mm. As a result, a single antenna becomes inefficient in transmitting signals with enough power to communicate with nearby receivers and cannot be used on its own. A promising approach to overcome this difficulty relies on an array of spatially distributed antennas transmitting synchronous signals. Depending on the application, some antennas will be required to transmit fully coherent signals, while others may be required to transmit signals with specific phase delays. In both cases, the precise control over the frequency and phase of the transmitted signals is important. The aim of this work is to develop the concept of Phase-Locked Loop (PLL) and Delay-Locked Loop (DLLs) networks capable of generating stable, distributed and coherent clocking signals for synchronous signal transmission, i.e., frequency synthesis for 5G. The project will focus on the system-level design, functionality test on field-programmable gate arrays (FPGA) and the study of the feasibility of the concept for on-chip implementation for frequencies over a GHz range.
Location	University College Dublin
Experience	The PhD position is funded for 4 years, including a monthly stipend and a travel budget to present at international conferences, workshops and seminars. The successful candidate will be hosted at the School of Electrical and Electronic Engineering, University College Dublin (Ireland) and will work in the Circuits and Systems Research Group. The successful applicant must hold an Honours Master's (preferably) or Bachelor Degree (Level 8) with a performance equivalent to at least a second class upper division Honours in Electronic Engineering, Applied Physics or Computer Science. The candidate must have excellent knowledge of control theory, electronic circuits, statistics, dynamical systems, complex systems and networks. Practical experience in software development, computer simulation and modelling is essential. It is

	expected that the candidate will have excellent communication skills and the ability to work well in an interdisciplinary team.
Funding / Stipend	The studentship will cover fees up to 5,500k pa and a stipend of 18,500k pa
Closing Date	30th June 2018
Contact	Dr. Elena Blokhina, elena.blokhina@ucd.ie
Application Process / Additional Information	Interested candidates should apply by email to Dr. Elena Blokhina elena.blokhina@ucd.ie. Early applications are encouraged. Applications should include: 1) a cover letter (1 page) explaining their interest in the project topic and mentioning any relevant background and/or experience; 2) a Curriculum Vitae. Academic transcripts and two academic references will be required after a shortlisting process takes place.